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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,288	04/20/2004	Kazuo Sakamoto	XA-10084	2625

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

NOTIFICATION DATE	DELIVERY MODE
09/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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MN

Office Action Summary	Application No.	Applicant(s)	
	10/827,288	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 6/29/2007.

2. Claims 1, 3-5, 9-10 have been amended, no claim has been added, claim 6 has been canceled. Thus, claims 1-5, 7-11 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 5, 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent Application Publication 2005/0243635), in view of Clark (US Patent 6650589).

For claim 1, Schaefer teaches the following limitations:

A data processing device (140, 120, 122, 124 in Fig 1) formed as a semiconductor integrated circuit, which is coupled to a device (112) for performing data transmission and reception (112 is a memory that transmits and receives data), said data processing device comprising: a central processing unit (140); an interface unit (200 and the clock distribution network to DQ buffers) for data transmission and reception to and from the external device, wherein said interface unit includes: an external terminal (terminal for CLKD in Fig 2) for outputting a clock signal; an output driver for driving said external

terminal to output said clock signal (the wires connecting CLKD to 212a-212i in Fig 2 form clock distribution network and can be considered as output driver as the network is driving the terminal to provide clock to DQ buffers); a load circuit (210, 204, 206, 208) capable of imparting, to the clock signal (202) extracted from a position in a stage previous to output driver in a clock signal path (210 extracting signal just before CLKD in Fig 2), a variable delay ([0005] mentions that delay compensation circuit compensate for variations in process temperature, loading conditions. Thus, circuitry within 200 incorporates a variable delay) in accordance with a delay (delay = B) resulting from an external load (DQ buffers shown in 212a-212i) coupled to external terminal in order to generate a delayed clock signal (CLKD is a delayed signal) for latching data inputted from the external device (CLKD is applied to C input of buffers and data D is latched to 213a-213i from 212a-212i, 213a-213i), wherein both the output driver and the load circuit operate at the same voltage voltage ([0013] mentions that delay calibration, compensation and control, as well as memory array, are within 110. Thus, both output driver and load circuit are within 110. Fig 1 shows that 110 is driven by one voltage Vcc. Therefore, output driver and load circuit operates at the same voltage).

Although 112, a DRAM memory array ([0013]), is shown within 110, it can be placed as an external unit as DRAM can be a stand alone device in an integrated circuit. One ordinary skill would be motivated to use 112 as an external device as it provides the modular design.

Schaefer does not mention that CPU operating voltage is lower than that of output driver and load circuit.

Clark teaches that a microprocessor core has lower operating voltages than that of a memory device (lines 25-34 of column 3). Since, output driver and load circuit of Schafer have same operating voltage as memory array (Fig 1), the output driver and load circuit of Schaefer can be operated at a second voltage higher than CPU operating voltage.

It would have been obvious to one ordinary skill in the art to combine the teachings of Schaefer and Clark to operate load circuit and output driver operating at second voltage higher than CPU voltage, since such a system ensures CPU voltage to go down with stable memory operation (lines 20-25 of column 1).

For claim 4, Schaefer teaches the following limitations:

A data processing device (140, 120, 122, 124 in Fig 1) formed as a semiconductor integrated circuit, which is coupled to a memory device (112) for performing data transmission and reception (112 is a memory that transmits and receives data and controller 120 controls operation of memory; [0013]), said data processing device comprising:

a central processing unit (140); a clock pulse generation circuit capable of generating different clock pulse signals (510 in Fig 5b shows the pulses of clock. Therefore, there is

clock generation circuit); and an interface unit (200 and the clock distribution network to DQ buffers) for data transmission and reception to and from the external memory device ([0014] mentions that delay compensation circuit is for use with memory), wherein said interface unit includes:

a first external terminal (terminal for CLKD in Fig 2) for outputting a clock signal (CLKD) derived from a clock pulse signal (202) generated by the clock pulse generation circuit;

an output driver for driving said first external terminal to output said clock signal (the wires connecting CLKD to 212a-212i in Fig 2 form clock distribution network and can be considered as output driver as the network is driving the terminal to provide clock to DQ buffers); and

a load circuit (210, 204, 206, 208) capable of imparting, to the clock signal extracted from a position in a stage previous to said output driver in a clock signal path (210 extracting signal just before CLKD in Fig 2), a variable delay ([0005] mentions that delay compensation circuit compensate for variations in process temperature, loading conditions. Thus, circuitry within 200 incorporates a variable delay) in accordance with a delay (delay = B) resulting from an external load (DQ buffers shown in 212a-212i, 213a-213i) coupled to said first external terminal, wherein both the output driver and the load circuit operate at the same voltage voltage ([0013] mentions that delay calibration, compensation and control, as well as memory array, are within 110. Thus, both output driver and load circuit are within 110. Fig 1 shows that 110 is driven by one voltage Vcc. Therefore, output driver and load circuit operates at the same voltage).

Although 112, a DRAM memory array ([0013]), is shown within 110, it can be placed as an external unit as DRAM can be a stand alone device in an integrated circuit. One ordinary skill would be motivated to use 112 as an external device as it provides the modular design.

Schaefer does not mention that CPU operating voltage is lower than that of output driver and load circuit.

Clark teaches that a microprocessor core has lower operating voltages than that of a memory device (lines 25-34 of column 3). Since, output driver and load circuit of Schafer have same operating voltage as memory array, the output driver and load circuit of Schaefer can be operated at a second voltage higher than CPU operating voltage.

It would have been obvious to one ordinary skill in the art to combine the teachings of Schaefer and Clark, since such a system ensures CPU voltage to go down with stable memory operation (lines 20-25 of column 1).

For claim 5, 212a-212i, part of DQ buffers (explained in [0005]), comprises latch circuits for receiving data through external terminals D0-D1 from memory array, which are clocked by clock signal as delayed by load circuit to latch the data.

However, the latch circuits do not operate in first voltage in Schaefer. In Clark's system, latch circuits 50 operate at first voltage to latch data to the CPU (lines 14-21 of column 4). One ordinary skill would be motivated to operate latch circuits in first voltage, since data needs to be converted to CPU compatible voltage.

For claim 9, 207 of Schaefer comprises a selector circuit to selectively pass the external clock signal through the appropriate delay components ([0015]), which can be though as time constant circuits, to latch the data from the memory. 200 operates in one voltage Vcc, and therefore 207 operates in second voltage.

For claim 10, 400 is the register that determines power control mode ([0024]). 207 effects that power saving mode ([0015]). Thus, the circuit comprises a register to store the value for the selector and a decoder necessary to generate the control signals for the selector in accordance with the set value. [0024] mentions that 400 can be part of other control circuit. Therefore, EMR can be operated with CPU voltage, while the decoder generating control signal can be part of 200 and operates in second voltage.

4. Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent Application Publication 2005/0243635), in view of Clark (US Patent 6650589), further in view of Grossnickle et al (US Patent Application Publication 2004/0064749).

For claims 2, 3, 7 and 8, Schaefer and Clark do not teach that the load circuit is a time constant circuit comprising resistors and capacitors.

Grossnickle et al teach the delay circuit comprising resistors (P1301) and capacitors (CAP0-CAP3). Fig 3 shows the delay circuit comprising time constant circuits for generating signals with different amounts of delay. Grossnickle et al generate plurality of clock signals with different amount of delay ([0027] mentions that clock generators and delay lock loops use delay elements to manipulate clock edges. Thus, clock generators, DLLs generate plurality of delayed clock signals). Clock signals are typically used to latch data in memory, buffers, registers and other storage units, where any of the clock signals generated from clock generators, DLL, PLL can be selected for latching data inputted from external device.

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Schaefer, Clark and Grossnickle. One ordinary skill in the art would be motivated to have the time constant circuits as taught by Grossnickle in the system of Schaefer to tune the delay settings.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent Application Publication 2005/0243635), in view of Clark (US Patent 6650589), further in view of Strub et al (US Patent Application Publication 2004/0156616).

For claim 11, Schaefer teaches the data processing device as stated above. In addition, Schaefer teaches memory array 112 coupled to data processing device that performs data transmission and reception based on clock signal outputted from external terminal of said data signal. However, Schaefer does not teach any non-volatile storage as 112 is a DDR ([0013]).

Strub et al teach a non-volatile storage device that is controlled by DDR ([0141] of page 18). Therefore, non-volatile storage is based on DDR, which in turn based on clock signal outputted from external terminal of said data processing device. Thus, non-volatile storage is based on clock signal outputted from external terminal of said data processing device.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Schaefer, Clark and Strub et al. One ordinary skill would be motivated to control non-volatile through DDR, since that can effect in power saving ([0141] in Strub et al).

Response to Arguments

Applicant's arguments filed on 6/7/2007 have been considered but are moot in view of the new ground(s) of rejection.

However, Schaefer is still relied upon for rejection and Examiner is addressing arguments regarding Schaefer.

Applicant argues that Schaefer does not teach output driver and load circuit to operate at same voltage.

Examiner disagrees. [0013] mentions that delay calibration, compensation and control, as well as memory array, are within 110. Thus, both output driver and load circuit are within 110. Fig 1 shows that 110 is driven by one voltage Vcc. Therefore, output driver and load circuit operates at the same voltage

Conclusion

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman
Examiner
Art Unit 2116

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REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
9/17/07